Description

2263-63Nis highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter up to 60W output power system.

PWM switching frequency is internally fixed at 65KHz. At no load or light load condition, the IC operates in 'burst mode' to minimize switching dissipation. Therefore, lower standby power dissipation and higher conversion efficiency are achieved.

Due to very small startup current and low operating current, a big resistor can be used in the startup circuit to minimize standby power dissipation.

2263-63Noffers comprehensive protection functions, including Cycle-by-Cycle current limitation (OCP), over temperature protection (OTP), Over voltage clamp (OVP)and under voltage lockout (UVLO) on VDD. The Gate output is clamped up to 16V to protect the gate of the power MOSFET.

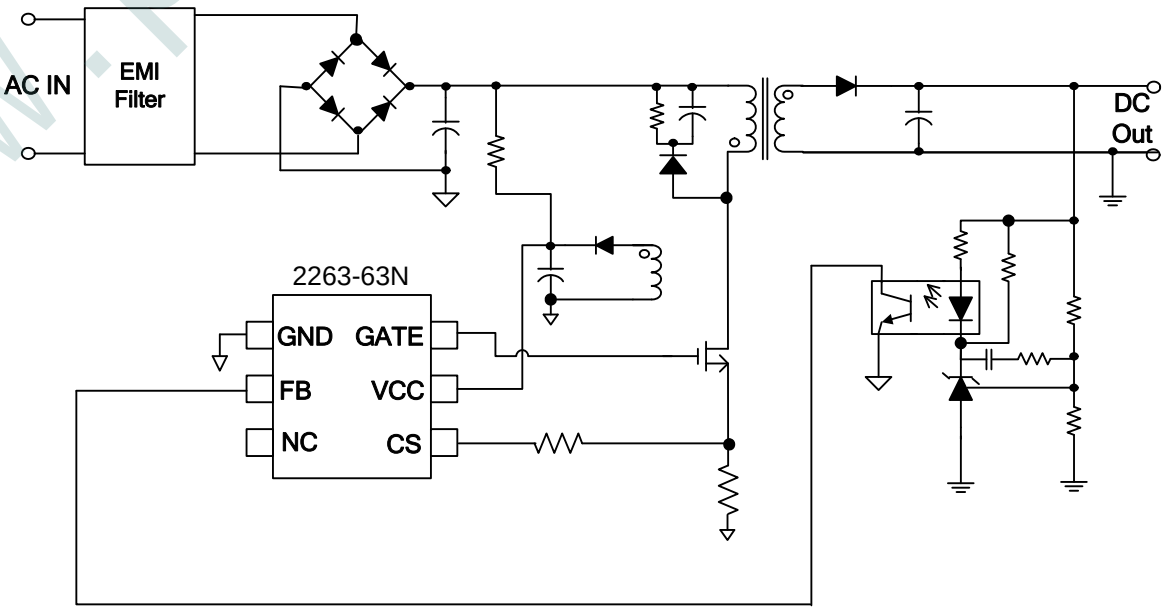
Features

- Digit frequency shuffling technology to improve EMI performance.
- Leading-edge blanking on current sense input.
- Slope compensation.
- Burst mode control to improve efficiency and optimize standby power dissipation.
- Low startup current and low operating current.
- Voltage clamping at gate output
- Soft-start to reduce MOSFET stress during power on.
- Comprehensive protection functions
  1、Under voltage locked with hysteresis (UVLO) on VDD
  2、Over voltage protection (OVP) on VDD.
  3、Cycle-by-Cycle current limitation
  4、Current limitation compensation to obtain the same output current in universal ac line input
  5、Over load protection (OLP)
  6、Over temperature protection (OTP)
- 300mA drive capability

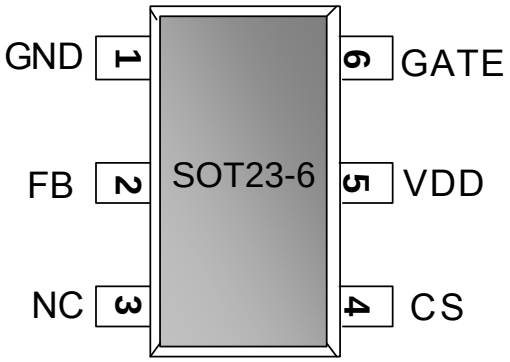
Applications

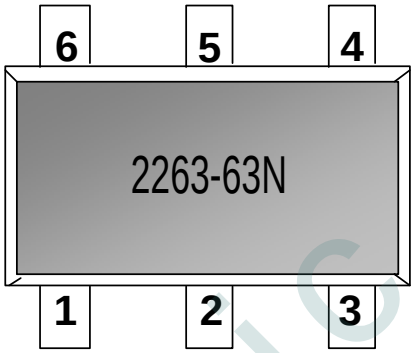
- Cell Phone Charger
- Digital Cameras Charger
- Power adaptor
- Battery charger

Application Circuit

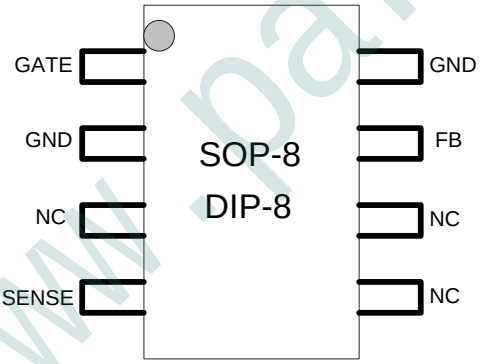


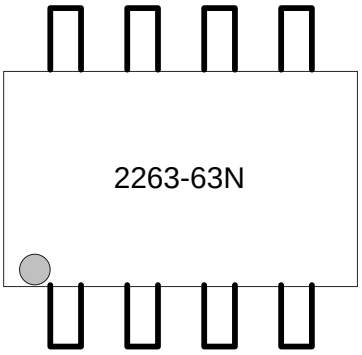
Pin Assignment & Marking Information





Y:	Year code (2018=J)
WW:	week code (01-52)
ZZZ:	LOT NO
G:	Wafer code
H:	FAB code





H:	Wafer code
Y:	Year code (2018=J)
WW:	week code (01-52)
ZZZ:	LOT NO
K:	FAB code

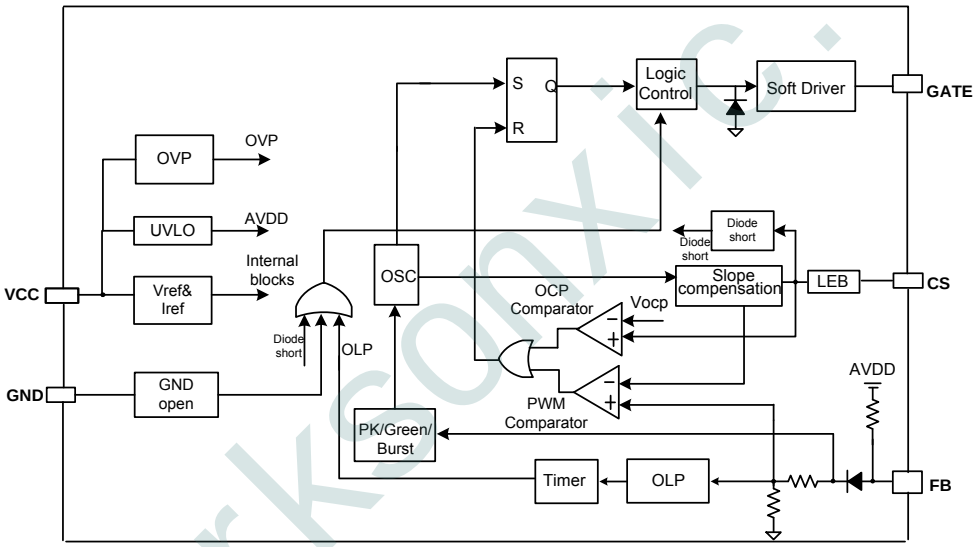
Ordering Information

Part number	Package	MOQ(PCS)
2263-63N	SOT23-6	3000
2263-63N	SOP-8	4000
2263-63N	DIP-8	2000

Pin Description

Symbol	Type	Description
GATE	O	Totem-pole gate dive output for the power MOSFET
VDD	P	Chip DC power supply pin
SENSE	I	Current Sense input pin.
FB	I	Feedback input pin.
GND	P	Ground.

Block Diagram



Absolute Maximum Rating

Parameter	Value	Unit
VDD supply voltage	27	V
VDD clamp voltage	29	V
VDD clamp current	10	mA
VFB input voltage	-0.3 to7	V
VSENSE input voltage to SENSE pin	-0.3 to7	V
Min/Max operating junction temperature	-55 to 150	℃
Operating ambient temperature	-20 to 85	℃
Thermal resistance, Junction to shell SOT23-6	250	℃/W

Note: Stresses above absolute maximum ratings may cause permanents damage to the device. Exposure to absolutely maximum-rated conditions for extended periods may affects device reliability

Recommended Operating Conditions

Symbol	Parameter	Min. Max.	Unit
VDD	Supply Voltage Vcc	9 to 25.5	V
T_{OA}	Operating Ambient Temperature	-20 to 85	℃
ESD-HM	Human Model	2	KV
ESD-MM	Machine Model	150	V

Electrical Characteristics(T_A = 25 ℃, if not otherwise noted)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Supply Voltage(V_{dd} Pin)						
Idd_startup	VDD start up current	VDD=12.5V		3	15	uA
Idd	VDD operation current	VDD=16V ， FB=3V			2.3	mA
UVLO(ON)	VDD under voltage lockout enter		6.8	7.8	8.2	V
UVLO(OFF)	VDD under voltage lockout exit		13	13.4	16.5	V
VDD_OVP	VDD over voltage protection		25.5		28	V
Voltage Feedback (FB Pin)						
AVCS	PWM input gain	ΔVFB/ΔVSENSE		2		V/V
VFB_open	VFB open loop voltage			5.7		V
IFB_short	FB pin short current	Short FB pin to GND and	0.6	0.8	1	mA
VFB_burst	Burst mode voltage			1.1		V
VTH_PL	Power limiting FB threshold voltage		2	3.7		V
TD_PL	Power limiting delay time			120		mS
DC_MAX	Maximum duty cycle	VDD=18V, FB=2.0V		75		%
Current Sensing (SENSE Pin)						
T_blanking	Leading-edge blanking time		120	250	750	nS
ZSENSE_IN	Input impedance			40		KΩ
VTH_sense	Over current threshold voltage	Duty=0	0.74	0.8	0.86	V
Oscillator						
Fosc	Normal oscillation frequency		62	68.5	75	Khz
Δf_temp	Frequency temperature stability	VDD=16V TA =-20℃ to		5		%
Δf_VDD	Frequency voltage stability	VDD=12V to 25V		5		%
Fosc_BM	Burst mode base frequency		17	20	28	Khz
Δf_OSC	Frequency modulation range /Base		-5		+5	%
Gate Drive Output						
VOL	Output low level	VDD=16V, IO=-20mA			0.8	V
VOH	Output high level	VDD=16V, IO=20mA	10			V
V_Clamp	output clamp voltage level			16		V
T_r	Output rising time	VDD=16V, CL=1nF		220		nS
T_f	Output falling time	VDD=16V, CL=1nF		70		nS

Application Information

2263-63Nis a highly integrated PWM controller IC optimized for offline flyback converter up to 60W power system. The burst mode control greatly reduces the standby power consumption and helps the designer easily meet the international energy-saving requirements.

Startup Current and Startup Control

Startup current of 2263-63Nis designed to be very low so that VDD could be charged up above UVLO threshold level quickly. Therefore, a large value resistor can be used to minimize the power dissipation in application. For AC/DC adaptor within universal input range, a 2 MΩ, 1/2 W resistor could be connected to VDD capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The Operating current of 2263-63Nis lower 2.3mA. Therefore, 2263-63Ncan have a good efficiency.

Frequency shuffling for EMI improvement

The frequency Shuffling is implemented in 2263-63N.The oscillation frequency is modulated with a random source so that the harmonic energy is spread out. The spread spectrum minimizes the conduction EMI and therefore reduces system design challenge.

Burst Mode Operation

At zero load or light load condition, the main power dissipation in a switching mode power supply is from switching on the MOSFET, the transformer core and the snubber circuit. The magnitude of power dissipation is proportional to the number of switching frequency within certain period. Less switching frequency can reduce the power dissipation. 2263-63Nadjusts the switching frequency according to the loading condition. From light load to no load, the FB voltage drops. While the FB voltage is less than 1.1V, the gate pin output is disabled and kept low, while the FB voltage is higher than 1.2V, the gate output recovers to normal working mode. This is called “burst mode”. To reduce audio noise, the switching frequency will be kept higher than 20KHz in burst mode.

Oscillator Operation

The switching frequency is internally fixed at 65kHz. No external frequency setting components are required on PCB design.

Current Sensing and Leading-Edge Blanking

Cycle-by-Cycle current limitation is offered in 2263-63N.The switching current is detected by a resistor into the SENSE pin. An internal leading-edge blanking circuit chops off the SENSE voltage spike at initial so that the external RC filtering on SENSE pin is no longer required. The current limiting comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the voltage in the SENSE pin and the FB pin.

Internal Synchronized Slope Compensation

Slope compensation circuit adds voltage ramp onto the SENSE voltage according to PWM pulse width. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage. Slope compensation can help 2263-63Nobtain the same output current in universal ac input voltage.

GATE DRIVE

GATE pin of 2263-63Nhas 300mA drive current capabiliyt and the hgihest voltage is clamped at 16V. Therefore, the dissipation of conduction and switching in MOSFET is minimized.

Protection Controls

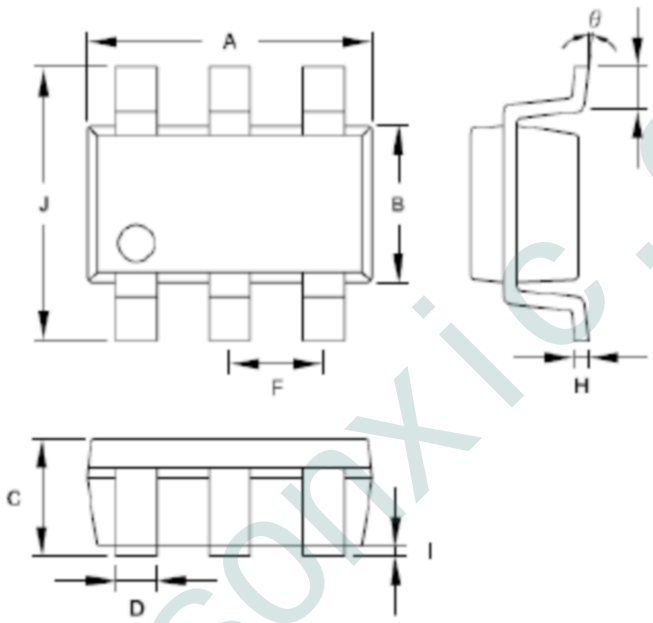
2263-63Nhas comprehensive protection functions including Cycle-by- Cycle current limitation (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP).

Current limitation compensation

To obtain the same output current capability, the OLP threshold voltage is compensated for the different input AC voltage. This function makes the current of OLP is in consistency whatever the AC input is (110V or 220V).

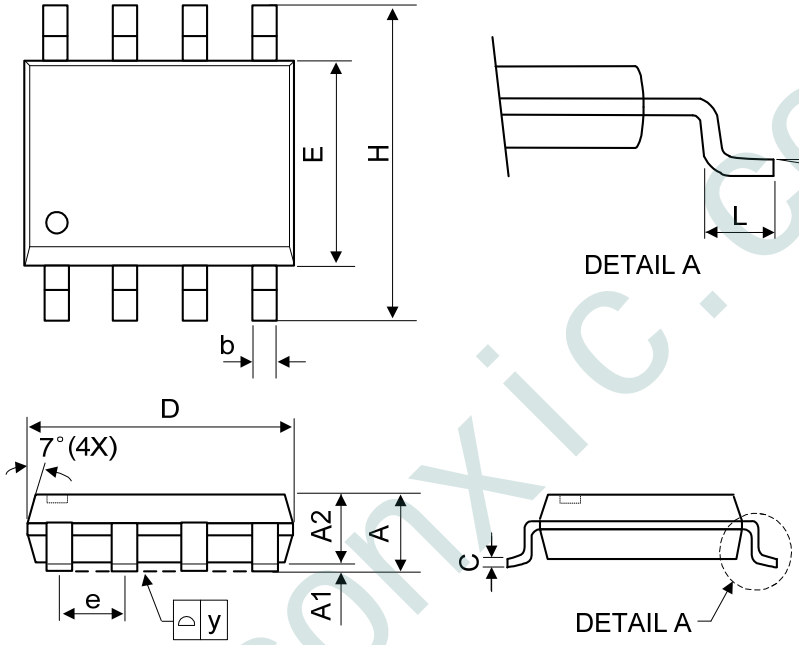
Package Information

SOT-23-6



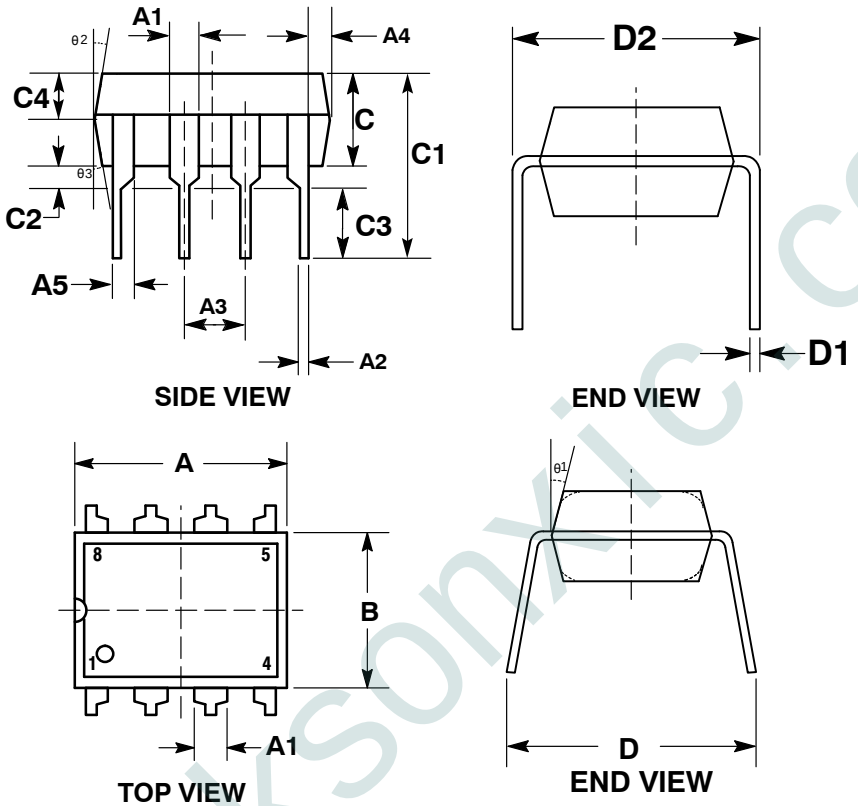
Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

SOP-8



SYMBOL	MILLIMETER			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.75	-	-	0.069
A1	0.1	-	0.25	0.04	-	0.1
A2	1.25	-	-	0.049	-	-
C	0.1	0.2	0.25	0.0075	0.008	0.01
D	4.7	4.9	5.1	0.185	0.193	0.2
E	3.7	3.9	4.1	0.146	0.154	0.161
H	5.8	6	6.2	0.228	0.236	0.244
L	0.4	-	1.27	0.015	-	0.05
b	0.31	0.41	0.51	0.012	0.016	0.02
e	1.27 BSC			0.050 BSC		
y	-	-	0.1	-	-	0.004
θ	0^O	-	8^O	0^O	-	8^O

DIP-8



SIZE / SYMBOL	MIN(mm)	MAX(mm)	SIZE / SYMBOL	MIN(mm)	MAX(mm)
A	9.00	9.2	C2	0.50TYP	
A1	1.474	1.574	C3	3.20	3.40
A2	0.41	0.51	C4	1.47	1.57
A3	2.44	2.64	D	8.20	8.80
A4	0.51TYP		D1	0.244	0.264
A5	0.99TYP		D2	7.62	7.87
B	6.10	6.30	Θ1	17° TYP	
C	3.20	3.40	Θ2	10° TYP	
C1	7.10	7.30	Θ3	8° TYP	

Revision History			
Version	**UPdate date**	**Version By**	**Revised content**
V0.9	**2018-7-14**	**Li Wen**	
V0.91	**2019-7-13**	**Li wen**	**OCP,OVP,LEB**