PULAN TECHNOLOGY CO., LIMITED

PL6650

Multi-Mode PWM Controller with Integrated Protections

Features

- Low Start-Up Current (<2.5uA)
- Multi-Mode Operation
  CCM @ Heavy Load and Low Line
  QR-Like Operation @ Medium Load
  Green mode with Valley Skip at Light Load
  Burst Mode at No Load
- Accurate Over Current Protection
- Adjustment OVP on QRD Pin
- Output Short Protection
- Soft Driver
- 8ms Soft-start
- OVP (Over Voltage Protection) on Vcc Pin
- On Chip OTP Protection
- SOT-26 Package with Few External Components Needed

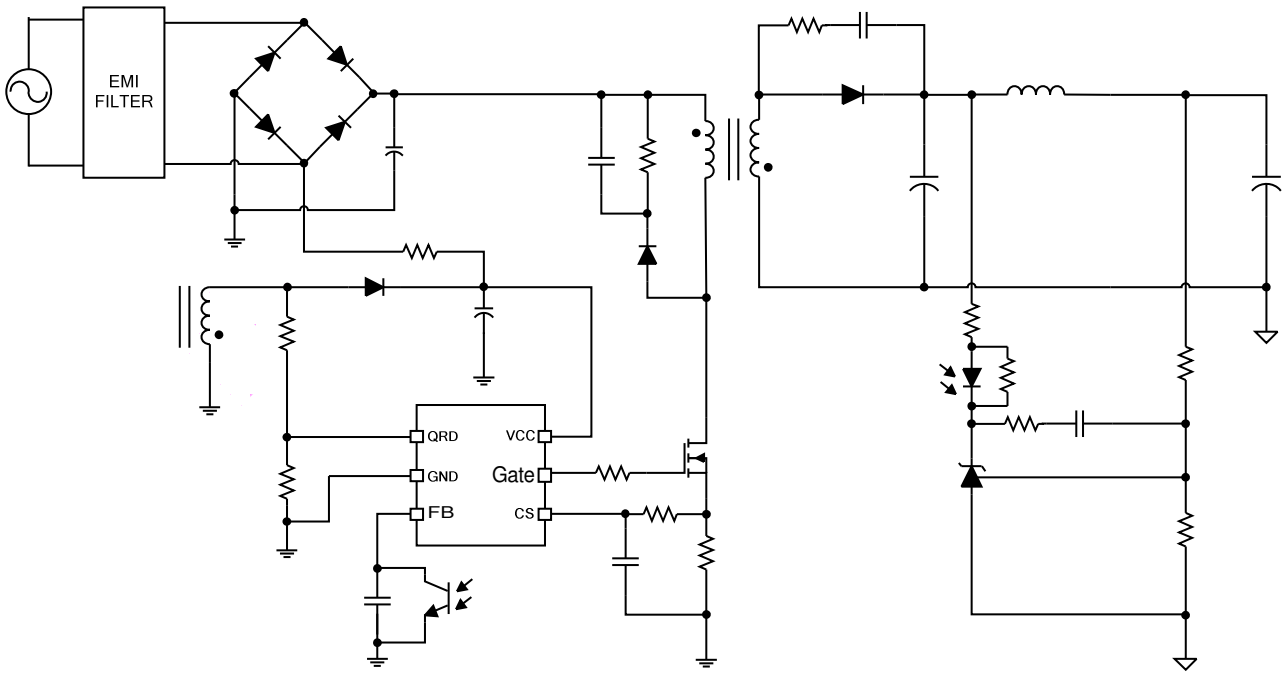
Description

The PL6650 is a high performance multi-mode (QR/CCM) PWM controller for flyback converter. It minimizes the components counts and is available in a tiny SOT-26 package. Those make it an ideal design for low cost application. It provides functions of low startup current, green- mode power-saving operation, VCC over-voltage protection, and QRD pin abnormal conditions sensing to prevent the circuit being damaged from the abnormal conditions.

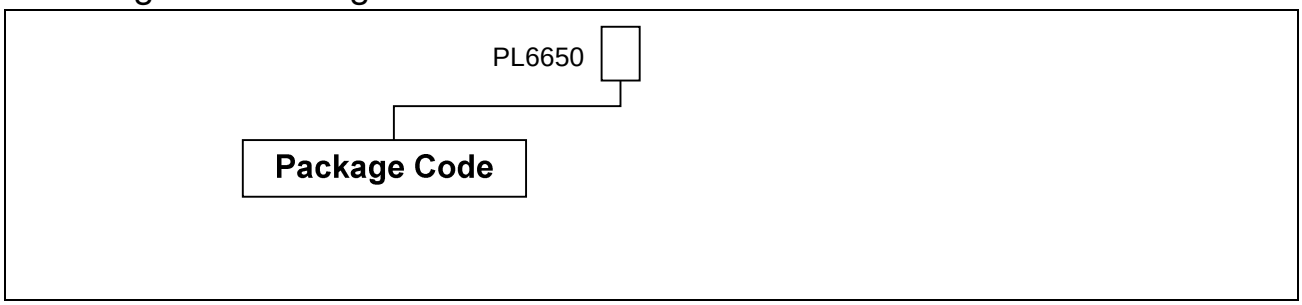
Applications

- Switching AC/DC power adapter
- SMPS Power Supply

Typical Application Information

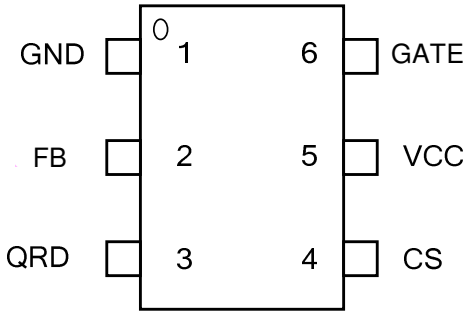


Ordering and Marking Information



Pin Configuration

SOT-26 (TOP VIEW)



Pin Description

Pin No.	Name	Function
1	GND	Ground reference pin
2	FB	Voltage feedback pin, by connecting a photo-coupler to control the duty cycle
3	QRD	This pin is for quasi-resonant detection and OVP.
4	CS	Current sense pin, connected to sense resistor for sensing the MOSFET current signal
5	VCC	Power supply pin
6	GATE	The output driver for driving the external MOSFET

Absolute Maximum Ratings

Supply voltage VCC ---------- 28V

FB, CS, QRD---------- -0.3~6.0V

GATE ---------- -0.3~Vcc+0.3V

Junction temperature ---------- 150℃

Storage temperature range ---------- -65℃ ~ 150 ℃

SOT-26 package thermal resistance ---------- 250℃/W

Power dissipation (SOT-26, at ambient temperature = 85℃) ---------- 250mW

Lead temperature (SOT-26 & DIP-8, soldering, 10 sec) ---------- 230℃

Lead temperature (All Pb free packages, soldering, 10 sec) ---------- 260℃

ESD, human body model ---------- 2.5KV

ESD, machine model ---------- 250V

Caution: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the IC. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The "Electrical Characteristics" table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction temperature	-20	125	℃
Operating ambient temperature	-20	85	℃
Start Up Resistor (AC Half side)	540k	2.2M	Ω
Supply voltage VCC	9.5	26.5	V
VCC Capacitor	2.2	10	μF
FB pin paralleling capacitor	1	33	nF
CS pin paralleling capacitor	100	1000	pF

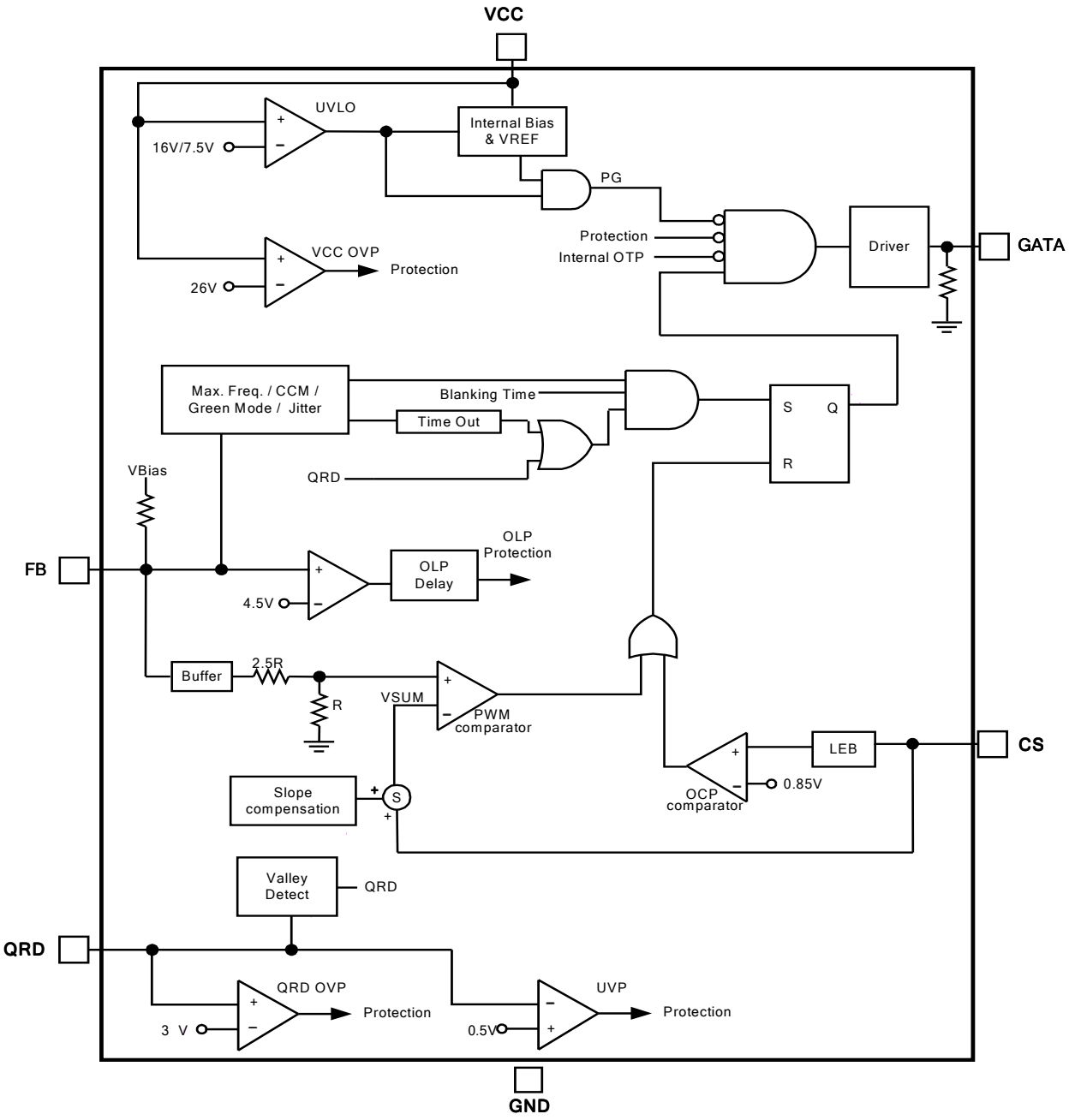
Note:

- Not to exceed the maximum junction temperature of the IC, this relates to the operating power of the IC and the thermal resistance of the IC-package as above.
- The small signal components should be placed to IC pin as possible.
- It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation.
- Connecting a capacitor to FBpin is also essential to filter out the undesired switching noise for stable operation.

Protection Mode

CCM Switching Frequency	OLP/UVP	VCC OVP	QRD OVP
65kHz	Auto recovery	Auto recovery	Auto recovery

Block Diagram



Electrical Characteristics (TA = +25℃ unless otherwise stated, VCC = 15.0V)

Parameter		Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE (VCC Pin)					
Startup current VCC=UVLO ON-0.1V		0.75	1.5	2.5	uA
Operating current (with 1nF load on GATE pin), Vcomp = 0V			0.65		mA
Operating current (with 1nF load on GATE pin), Vcomp = 2.5V			2		mA
Operating current (with 1nF load on GATE pin), protection tripped (VCC OVP, FB UVP)			0.65		mA
UVLO-OFF		7.0	7.5	8.0	V
UVLO-ON		15.2			V
VCC Mode Entry Point			8.5		V
Hysteresis			0.25		V
OVP level on VCC pin		24	26	28	V
OVP level on VCC pin Debounce Time*			128		μs
VOLTAGE FEEDBACK (FB Pin)					
Short circuit current, Vcomp = 0V			240		uA
Open loop voltage, FB pin open		4.8	5.2	5.6	V
Maximum Frequency Threshold, V_{SMAX}*			1.7		V
Green Mode Threshold*			1.35		V
Burst Mode Voltage		0.67	0.77	0.87	V
Hysteresis			100		mV
CURRENT SENSING (CS Pin)					
Maximum input voltage at Low Line, Vcsmax(ON Time>6us*)		0.80	0.85	0.90	V
Maximum input voltage at High Line, VcsmaxL (ON Time<5us*)		0.65	0.7	0.75	V
Internal Slope Compensation*			0.3		V
Leading-edge blanking time			350		ns
Input impedance		1			MΩ
Delay to Output*			100		ns
QRD (QRD Pin)					
Upper Clamp Level, IZCD=0.5mA			4.6		V
Lower Clamp Level, IZCD=-0.3mA			-0.3		V
QRD Blanking Time			2.5		μs
QRD OVP		2.85	3	3.15	V
OVP De-bounce Time*			128		μs
UVP Level			0.5		V
UVP De-bounce Time after start-up*			8		ms

Electrical Characteristics (TA = +25℃ unless otherwise stated, VCC = 15.0V)

Parameter		Min.	Typ.	Max.	Unit
OSCILLATOR					
CCM Frequency		60	65	70	kHz
Maximum Frequency Clamp, Vcomp>V_{SMAX}			69		kHz
Green Mode Frequency			25		kHz
Jitter Frequency (CCM, Vcomp>Vsmax)			±8		%
Soft Start Time (CS Pin)					
Soft Start Time*			8		ms
GATE DRIVER OUTPUT (GATE Pin)					
Output low level, VCC = 15V, Io = 20mA				1	V
Output high level, VCC = 15V, Io = 10mA		8			V
Output High Level, VCC=UVLO-OFF+0.2V		7		VCC	V
Rising time, load capacitance = 1000pF*			330		ns
Falling time, load capacitance = 1000pF*			45		ns
VGATE-clamp (VCC = 17V)			13.5		V
Maximum On Time (CCM Fs=70kHz)			10.8		μs
Open Loop Protection (FB Pin)					
OLP trip level, Vcomp			4.35		V
OLP delay time after start-up			64		ms
Internal OTP (Guaranteed by design)					
OTP*			145		℃
Hysteresis*			30		℃

*Guaranteed by Design.

Typical Performance Characteristics

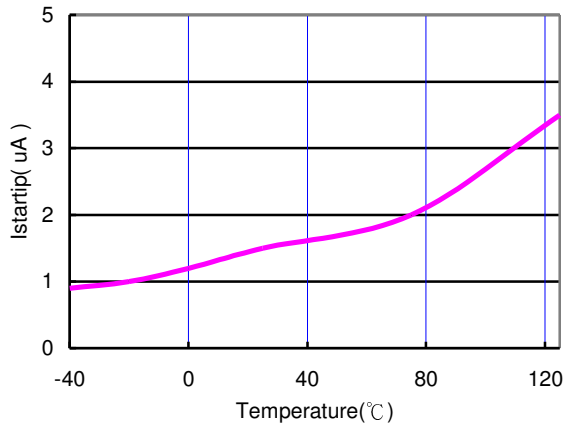


Fig. 1 Istartup current vs. Temperature

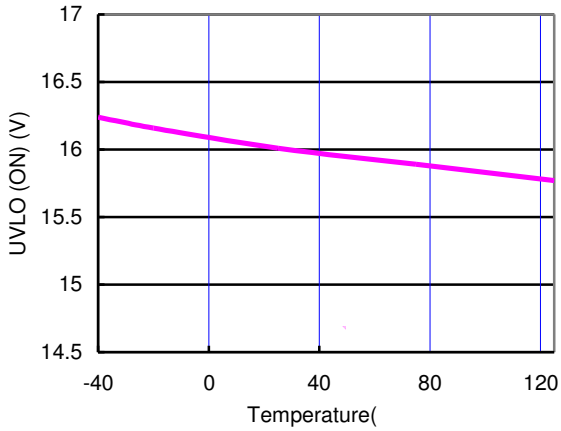


Fig. 2 UVLO (ON) vs. Temperature

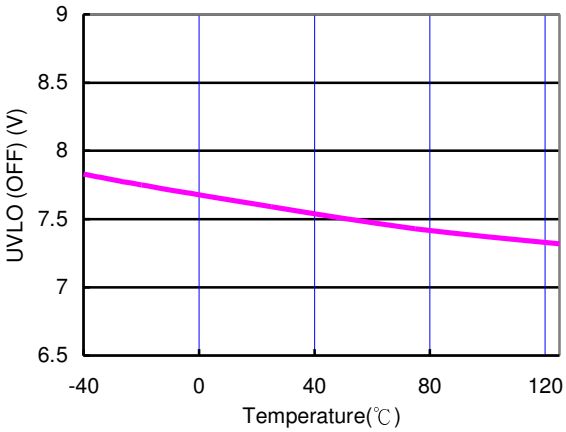


Fig. 3 UVLO (OFF) vs. Temperature

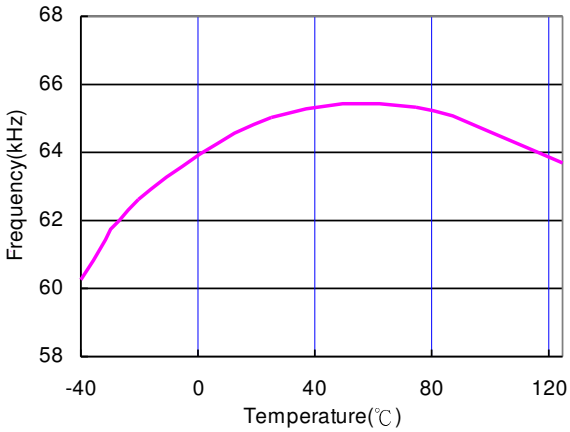


Fig. 4 Frequency vs. Temperature

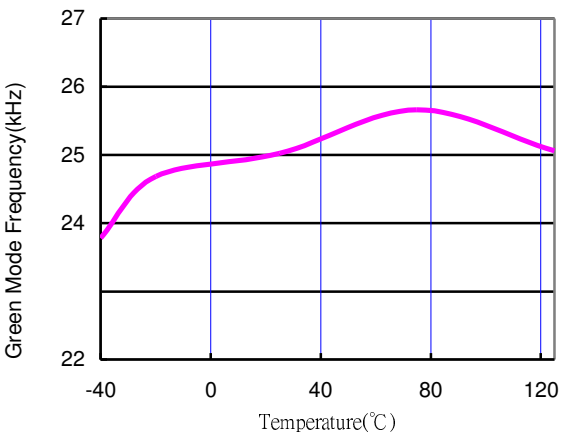


Fig. 5 Green Mode Frequency vs. Temperature

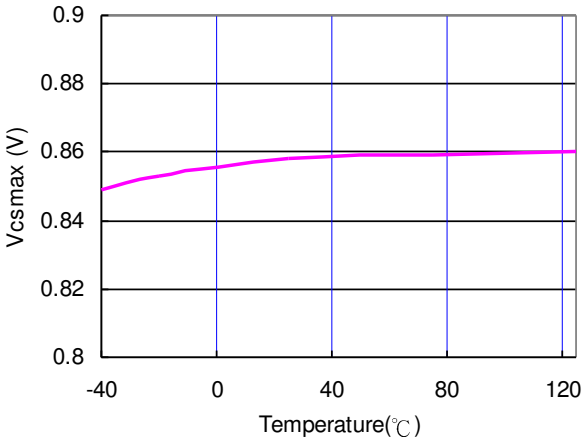


Fig. 6 Vcsmax vs. Temperature

Typical Performance Characteristics

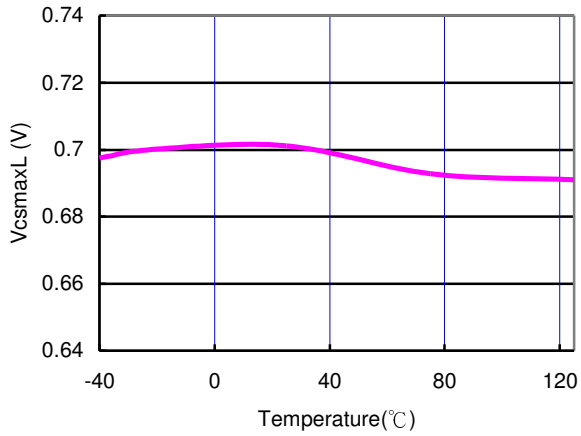


Fig. 7 VcsmaxL vs. Temperature

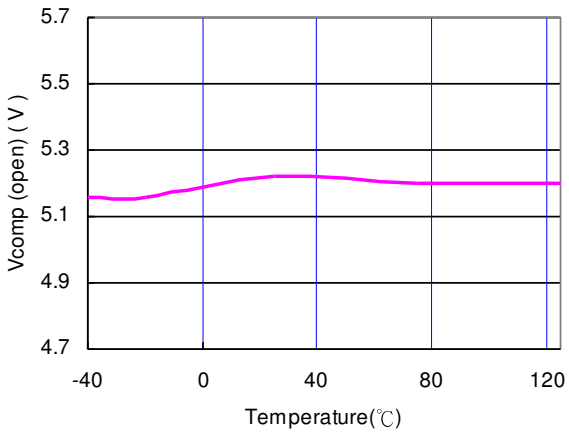


Fig. 8 Vcomp open loop voltage vs. Temperature

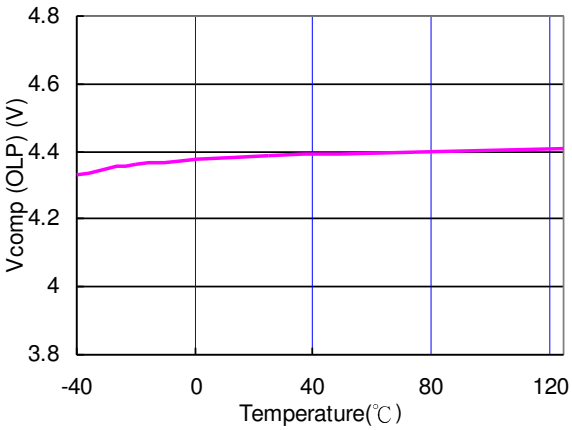


Fig. 9 Vcomp (OLP) vs. Temperature

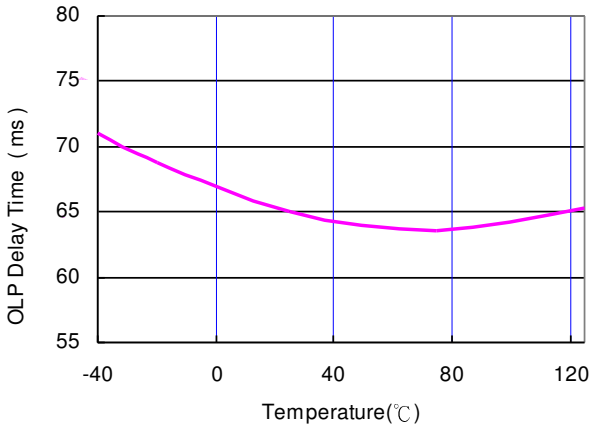


Fig. 10 OLP delay time vs. Temperature

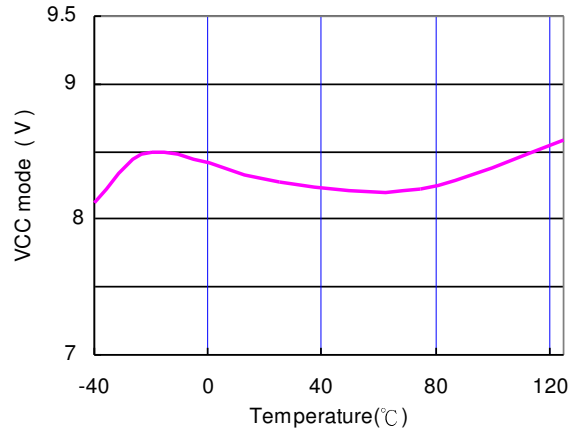


Fig. 11 VCC Mode (Entry) vs. Temperature

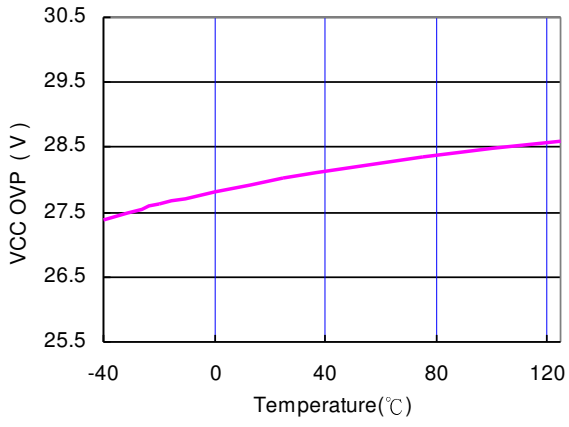


Fig. 12 VCC OVP vs. Temperature

Application Information

Overview

The PL6650 is a high performance multi-mode (QR/CCM) PWM controller for flyback converter. This results in a low-cost solution for low power AC/DC adapters. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Start-up Current

The typical start-up current is 1.5uA. Very low start-up current allows the PWM controller to increase the value of start-up resistor and then reduce the power dissipation on it.

Under-voltage Lockout (UVLO)

A hysteresis UVLO comparator is implemented in PL6650, then the turn-on and turn-off thresholds level are fixed at 16V and 7.5V respectively. This hysteresis shown in Fig.13 ensures that the start-u capacitor will be adequate to supply the chip durin start-up.

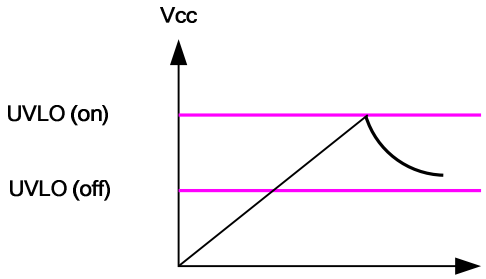


Fig.13

Multi-Mode Operation for High Efficiency

PL6650 is a multi-mode QR/CCM controller. The controller changes the mode of operation according to switching frequency and comp pin voltage, as shown in the Fig.14. At the normal operating condition, the IC operates in QR mode to reduce the switching loss. In the QR mode, the frequency varies depending on the line voltage and the load conditions. As the output load current is increased, the on-time T_{ON} is increased, and thus the switching frequency decreases. If the switching frequency lowers than 65kHz frequency, the controller adaptively transitions to a CCM mode. Thus, small size transformer can be used with high power conversion efficiency.

As the output load current is decreased, the on-time T_{ON} is decreased, and thus the switching frequency increases. If the switching frequency increases til over the clamp of 69kHz, IC will skip the first val to turn on in 2nd or 3rd valley.

At light load conditional, the VFB is lower than V_{SG1} and the system operates in green mode for high power conversion efficiency. The max switching frequency clamp will start to linearly decrease from 69kHz to 25kHz. The valley switching characteristic is still preserved in green mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced.

At zero load or very light load conditions (Vcomp< Burst mode voltage), the gate output pin of the PL6650 will be disabled immediately under such condition, enhancing power saving.

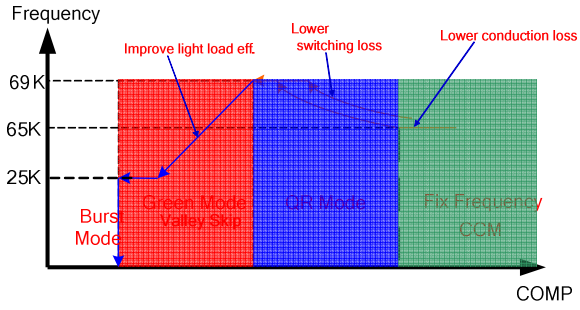


Fig.14

Quasi-Resonant Detection

The QR detection block will detect auxiliary winding voltage to turn on the MOSFET. The time-out2 generates a MOSFET turn-on signal as the driver output drops to low level for more than 150μs (Time GATE) with the falling edge of the driver output.

Leading-edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense resistor. To avoid fault trigger, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Internal Slope Compensation

A built-in slope compensation circuit is constructed in PL6650. When the switch is on, a ramp voltage is added to the sensed voltage across the CS pin, which helps to stabilize the system and prevent sub-harmonic oscillations.

Over-voltage Protection (OVP) on Auto

Recovery mode

To prevent power MOSFET from being damaged, the PL6650 is implemented an OVP function on VCC. When the VCC voltage is higher than the OVP threshold voltage, the output gate driver circu will be shut down immediately to stop the switching of power MOSFET. The VCC OVP function is an auto-recovery type protection. If OVP happens, the pulses will be stopped and recover at the next UVLO on. The PL6650 is working in a hiccup mode as shown in Fig. 15.

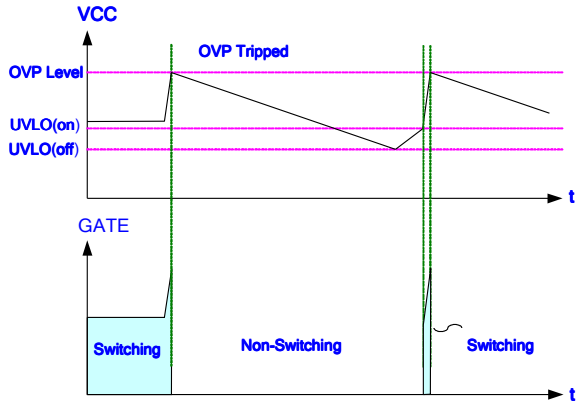


Fig.15

Output OVP on QRD - Auto Recovery mode

An output overvoltage protection is implemented in the PL6650, as shown in Fig. 16 and 17. It senses the auxiliary voltage via the divided resistors. The overvoltage protection works by sampling the plateau voltage after a delay time. The sampling voltage level is compared with internal threshold voltage 3.0V. If the sampling voltage exceeds the QRD OVP trip level, the QRD OVP circuit switches the power MOSFET off. The QRD OVP function is an auto-recovery type protection. The de-bounce time of QRD OVP is 128 s to prevent incorrect OVP detection which might occur during ESD or lightning events.

Output Under-voltage Protection (UVP) on QRD– Auto Recovery mode

To protect the circuit from damage due to output short condition, an auto-recovery type of UVP protection is implemented for it. If the QRD voltage declines below 0.5V for over the 8ms, the protection will be activated to turn off the gate until the next UVLO-ON.

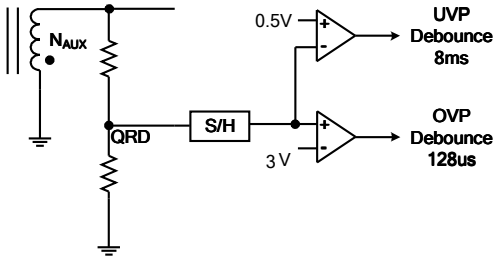


Fig.16

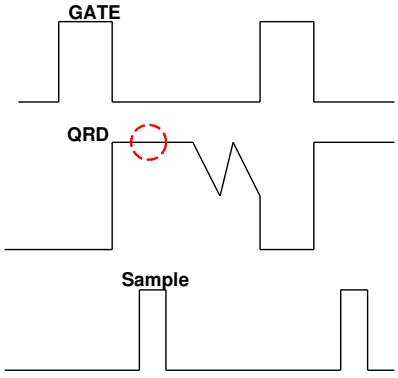


Fig.17

OLP (Open Loop Protection) – Auto Recovery mode

The PL6650 has open loop protection function. An internal circuit detects the Vcomp level, when the Vcomp is larger than an OLP threshold level and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit. Then VCC decreases below UVLO off level, the controller resets again.

Gate Clamp/Soft Driving

Driver output is clamped by an internal 13.5V clamping circuit to prevent from undesired over-voltage gate signals. And under the conditions listed below, the gate output will turn off immedia to protect the power circuit. The PL6650 also has soft driving function to minimize EMI.

VCC Mode Operation

In order to avoid the output voltage shut down by load changing from full to no load, the PL6650 is built-in the VCC mode function. When the load from full changes to no load, the output voltage will overshoot and pull low the FB pin by feedback loop (Into burst mode). Thus the duty will disappear and no power delivers to the secondary. If there is without any mechanism to prevent this situation, the VCC pin voltage will down to UVLO off and the IC will re-start again. In the PL6650, before the VCC is down to UVLO off, it will force the OUT pin outputs the specified duty to pull the VCC higher than UVLO off.

The VCC mode function is used to prevent the output re-start again when load changes. So never let the system operate on the VCC mode at no load. The system should operate on burst mode, otherwise the input power maybe become larger.

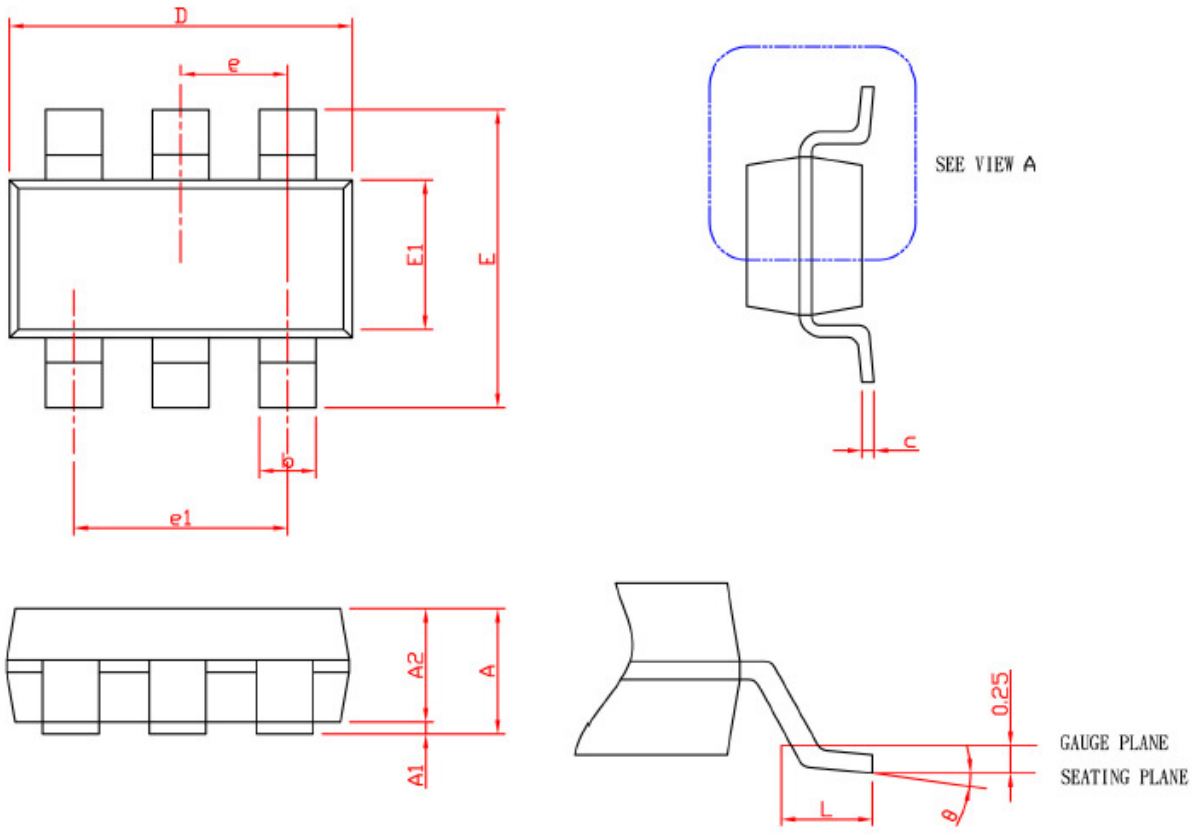
Fault Protection

There are several critical protections integrated in

CS pin floating
FB pin shorting
FB pin floating
QRD pin shorting

Package Information

SOT-26



SYMBOL	SOT-26			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note: 1. Followed from JEDEC MO-178 AB.

2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 10 mil per side