10-Bit DAC 120mA VCM Driver with I²C Interface

Description

The FP5510 is a single 10-bit DAC with 120mA output current voice coil motor (VCM) driver, with an I²C-compatible serial interface that operates at clock rates up to 400kHz. Its supply operates from 2.3V to 3.6V.

The FP5510 incorporates with a power-on reset circuit, power-down function. Power-on reset circuit ensure when supply power up, DAC output is to 0V until valid write bit value takes place. In power down mode, the supply current is about 1μA.

The FP5510 is designed for auto focus operation includes digital camera module, optical zoom camera phones and lens auto focus. The I²C address of FP5510 is 0x18h.

The FP5510 with WLCSP package which it is suitable for reduced-space mounting in mobile phone and other portable applications.

Features

- Power Supply Voltage Rang: 2.3V to 3.6V
- VCM Driver for Auto-Focus
- 10-Bit Resolution Current Sinking of 120mA for VCM
- 2-Wire I²C Interface (1.8V Interface Compatible)
- Internal 4 Slope Control Mechanism
  1. Enhance Slope Control Mode
  2. One Step Mode
  3. Linear Slope Mode
  4. Two Step Slope Mode
- Power-Save Mode Current < 1μA
- Power On Reset (POR)
- Small Size: 0.7mm×1.1mm (6-Balls WLCSP)

Applications

- Digital Camera Module
- Cell Phone
- Lens Cover
- Web Camera

Pin Assignments

6-Ball WLCSP

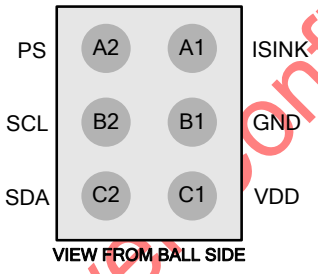


Figure 1. Pin Assignment of FP5510

Ordering Information

FP5510□

Package Type
E2: WLCSP (6-Ball)

WLCSP-6 (0.7mmx1.1mm) Marking

Part Number	Product Code
FP5510E2	2

Typical Application Circuit

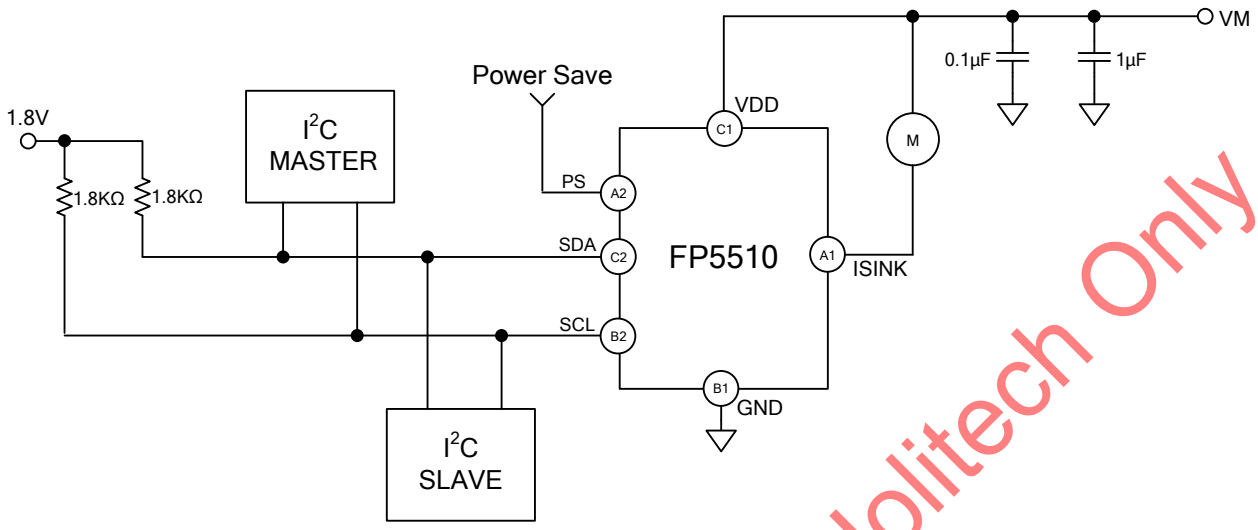


Figure 2. Typical Application Circuit of FP5510

Functional Pin Description

Pin Name	Pin No.	Pin Function
ISINK	**A1**	Output current sink.
PS	**A2**	Power save. Asynchronous power save.
GND	**B1**	Ground.
SCL	**B2**	I^2C interface clock signal.
VDD	**C1**	Power supply voltage.
SDA	**C2**	I^2C interface data signal.

Note:
PS: Power Save (Active Low)
1: Normal operation mode
0: Power save mode

Block Diagram

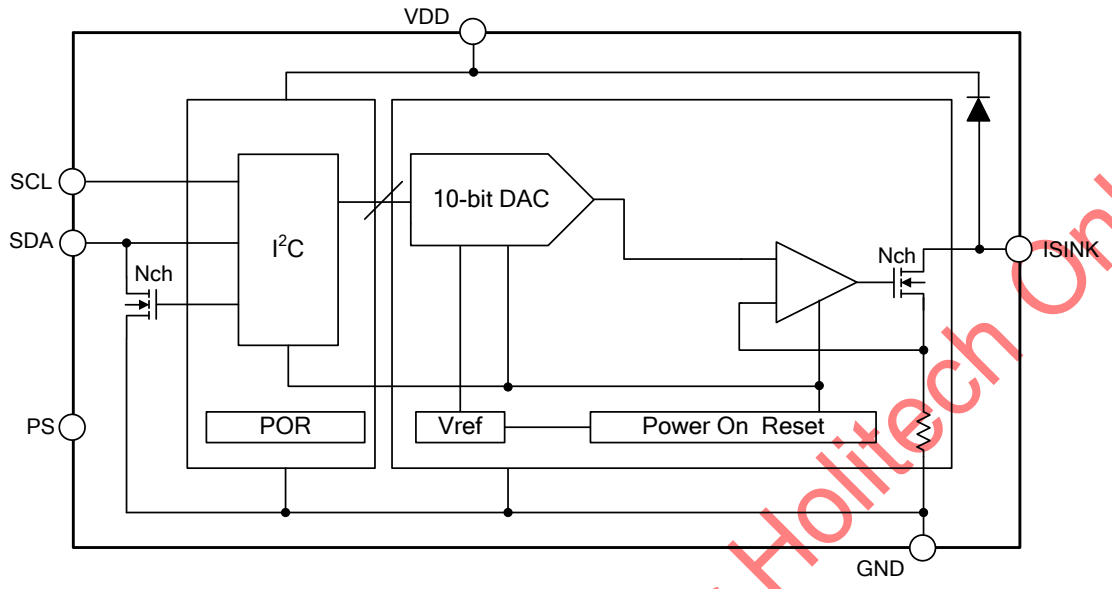


Figure 3. Block Diagram of FP5510

Absolute Maximum Ratings (Note 1)

- VDD to GND ---------- -0.3V to +4.5V
- SCL, SDA ,PS and ISINK to GND ---------- -0.3V to V_{DD}+0.3V
- Junction Temperature ---------- +150°C
- Storage Temperature Range ---------- -65°C to +150°C
- ESD (Human Body Model) ---------- 2000V
- ESD (Machine Model) ---------- 200V

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage, VDD ---------- +2.3V to 3.6V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(If not specified, V_{DD}=2.3V to 3.6V, V_{IN}=1.8V to V_{DD}, T_A=25°C).

Parameter	Conditions	Min	Typ.	Max	Unit
General Supply					
VDD		2.3		3.6	V
I_{SD}	Shutdown Mode (PS Pin Short to GND)	-1		+1	μA
I_{PD} (Power-Down Mode)	FP5510: PD=1 (Software)	-1		+1	μA
I_Q (Quiescent Mode)			0.3		mA
Power-on Time (Note 2)			12		mS
DAC Characteristics (V_{DD}=2.3V to 3.6V)					
DAC Resolution	117.3μA/LSB		10		Bits
LSB Relative Accuracy		-4		+4	LSB
LSB Differential Nonlinearity	Guaranteed Monotonic Over All Codes	-1		+1	LSB
Zero Code Error	All 0s Loaded to DAC	-1		+1	mA
Sink Current Characteristics					
Maximum Sink Current			120		mA
Output Voltage Range (Note 3)	Output Voltage Range Over which 100mA Sink Current is Available	150			mV
PS Logic Characteristics					
Input Current		-1		+1	μA
Input Low Voltage, V_{INL}	V_{DD}=2.3V to 3.6V			0.54	V
Input High Voltage, V_{INH}	V_{DD}=2.3V to 3.6V	1.26			V
2-wire Serial Interface Characteristics (SCL, SDA)					
Input Leakage Current, I_{IN}	V_{IN}=0V to V_{DD}	-1		+1	μA
Input Low Voltage, V_{INL}	V_{DD}=2.3V to 3.6V			0.54	V
Input High Voltage, V_{INH}	V_{DD}=2.3V to 3.6V	1.26			V
Glitch Rejection			50		ns

Note 2: FP5510 requires waiting time of 12ms after power on. During this waiting time, the offset calibration of internal amplifier is operating for minimization of output offset current.
Note 3: The output compliance voltage is guaranteed by design and characterization; not product tested.

I²C Interface Timing Specification

(Unless otherwise specified, V_{DD}=2.3V to 3.6V, all specifications form -40°C to +85°C).

Parameter	Min.	Max.	Description	Unit
f_{SCL}	0	400	SCL Clock Frequency	kHz
t_{HIGH}	0.6	-	Data Clock High Time	μs
t_{Low}	1.3	-	Data Clock Low Time	μs
t_r	$20+0.1C_b$ (Note 5)	300	SDA/SCL Rise Time	ns
t_f	$20+0.1C_b$ (Note 5)	300	SDA/SCL Fall Time	ns
$t_{HD:STA}$	0.6	-	Start Condition Hold Time	μs
$t_{SU:STA}$	0.6	-	Start Condition Setup Time	μs
$t_{HD:DAT}$ (Note 4)	0	0.9	Data Hold Time	μs
$t_{SU:DAT}$	100	-	Data Setup Time	ns
$t_{SU:STO}$	0.6	-	Stop Condition Setup Time	μs
t_{BUF}	1.3	-	Bus Release Time	μs
t_{SP}	0	50	Pulse Width of Spike Suppress	ns
C_b		400	Capacitive Load for Each Bus Line	pF

Note 4: A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
Note 5: C_b is the total capacitance of one bus line in pF, t_r and t_f are measured between $0.3V_{DD}$ to $0.7\ V_{DD}$.

I²C 2-Wire Serial Interface Timing Diagram

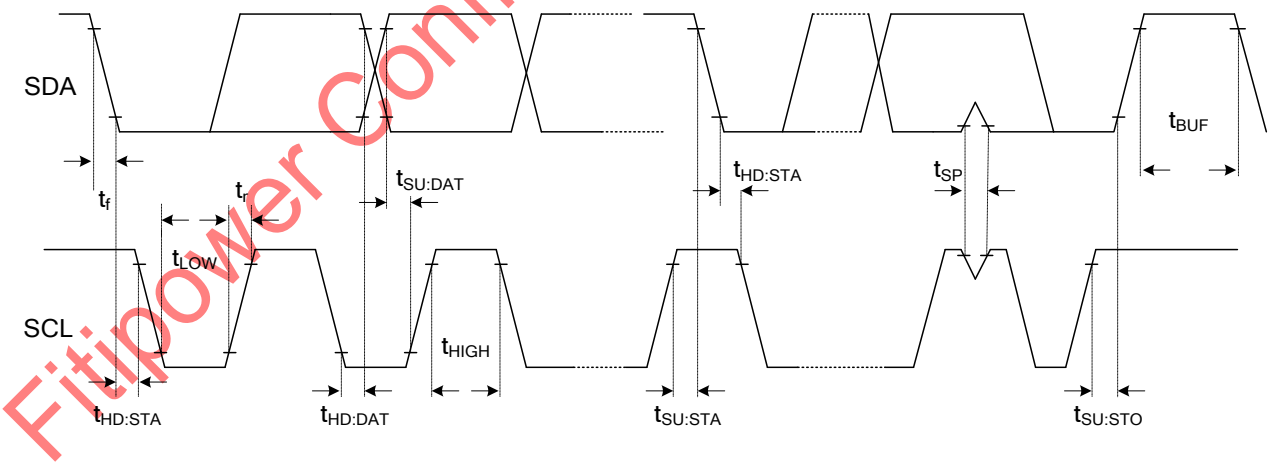
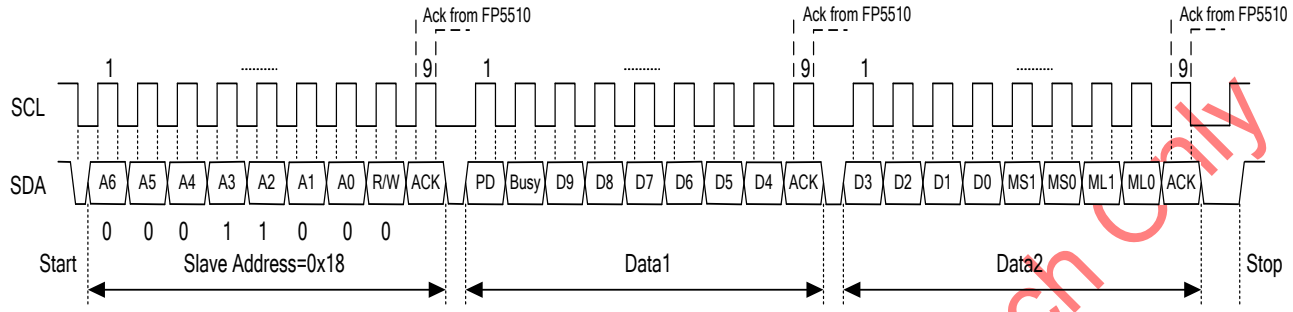


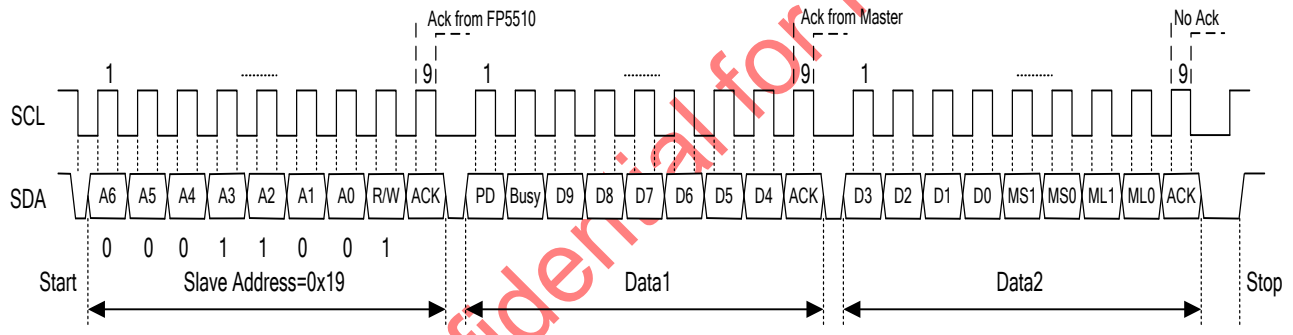
Figure 4. 2-Wire Serial Interface Timing Diagram

I²C Register Format

■ Write Operation



■ Read Operation



PD: Power Down Mode
1: Power down mode (active high)
0: Normal operation mode

Busy: Busy bit must keep “L” at writing operation

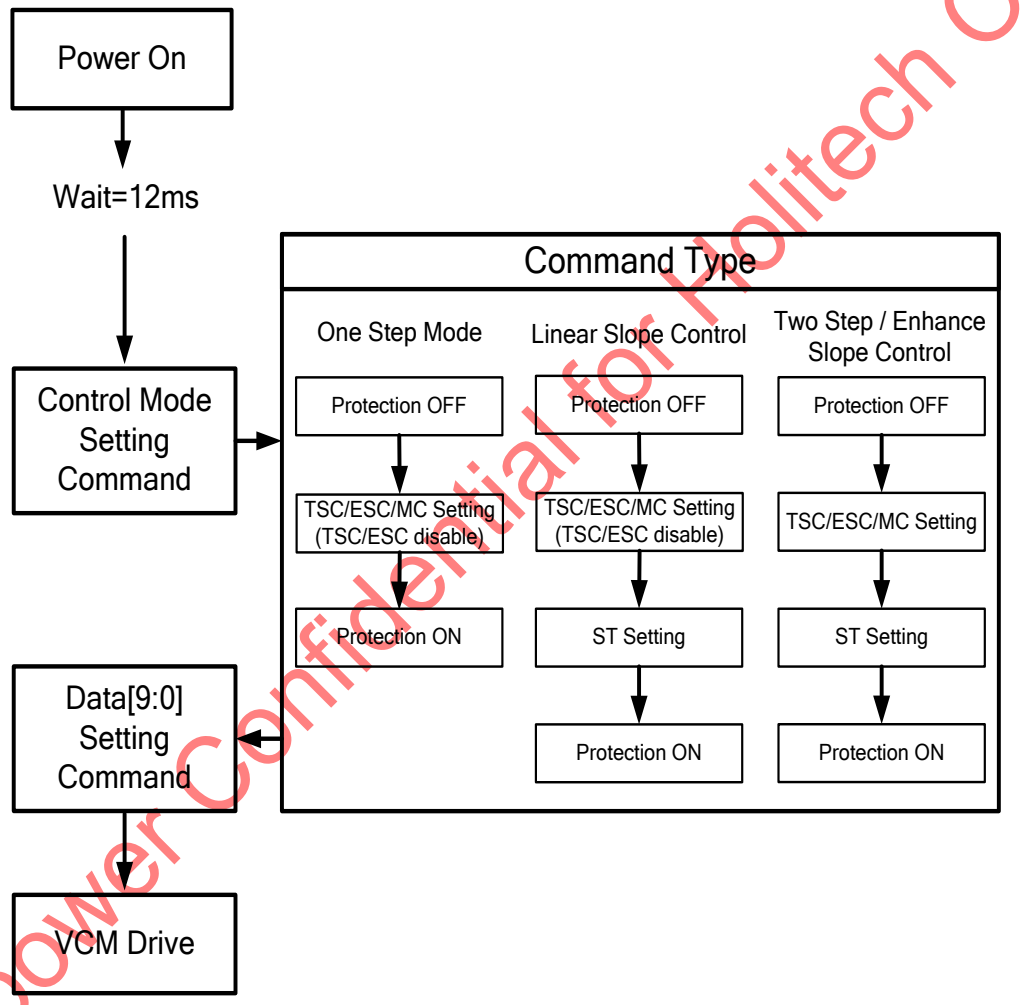
Read Operation:
Busy=1, it means that the Isink state is changing.
Busy=0, it means that the Isink state has been stable.

D[9:0]: Data Input
Output current= (D[9:0]/1023)×120mA
Max current= 120±5% (mA)

Application Information

1. Output Slope Control Set up Method

Internal 4 Slope Control Mechanism: One Step Mode, Linear Slope Control, Two Step Control and Enhance Slope Control.



※When you use one step mode after power on, you don't need register set. Because, TSC/ESC disable is default.

2. Linear Slope Control Set up Method

Protection off

Byte1(0xEC)								Byte2(0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

TSC, ESC and MC[1:0] setting

Byte1(0xA1)								Byte2							
1	0	1	0	0	0	0	1	0	0	0	ESC	TSC	1	MC1	MC0

ST[4:0] setting

Byte1(0xF2)								Byte2							
1	1	1	1	0	0	1	0	ST4	ST3	ST2	ST1	ST0	0	0	0

Protection on

Byte1(0xDC)								Byte2(0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

※When you use one step mode after power on, you don't need register set. Because, TSC/ESC disable is default.
※At one step mode and linear slope control, TSC and ESC code must be equal 0.

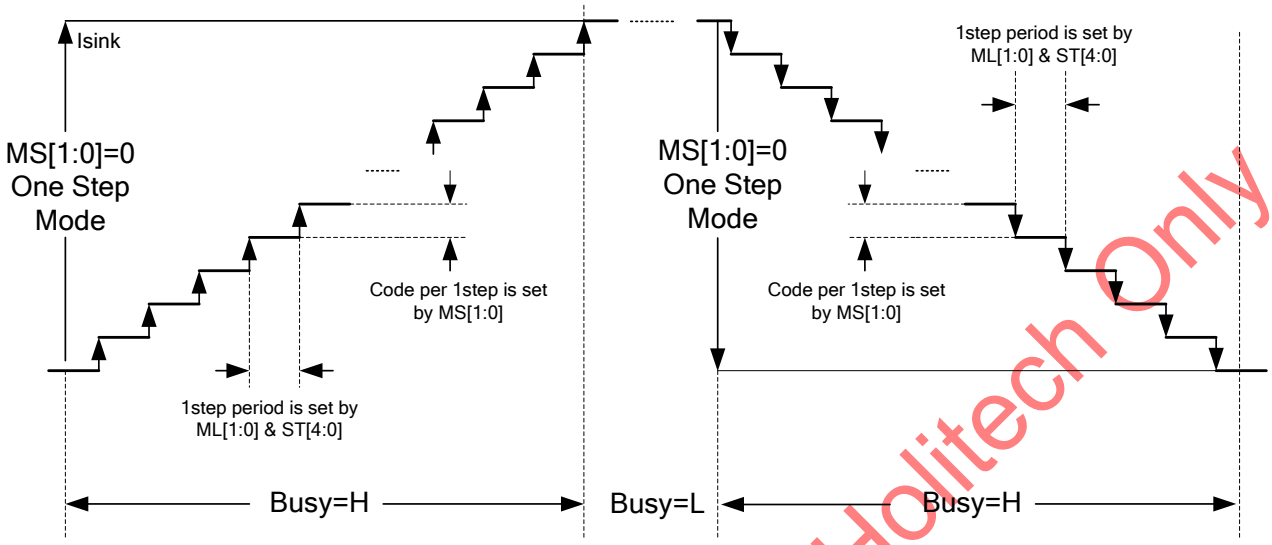
Linear Slop Control – step period selection table

Linear Slope Control step period is set by ML[1:0] and ST[4:0],

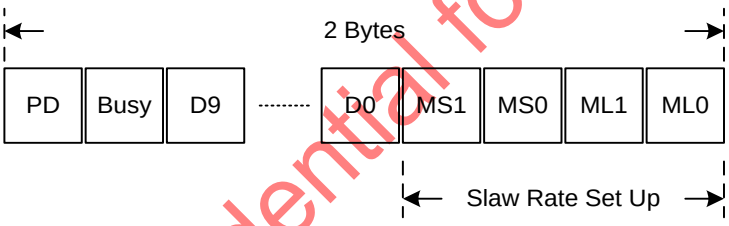
ST[4:0] default value is 5'b=00000 and ML[1:0] default value is 2'b=01. Unit[μs]

1 Step period				
ST[4:0], 5'b	ML[1:0], 2'b			
	00	01	10	11
10000	136.0	272.0	544.0	1088.0
10001	130.0	260.0	520.0	1040.0
10010	125.0	250.0	500.0	1000.0
10011	120.0	240.0	480.0	960.0
10100	116.0	232.0	464.0	928.0
10101	112.0	224.0	448.0	896.0
10110	108.0	216.0	432.0	864.0
10111	104.0	208.0	416.0	832.0
11000	101.0	202.0	404.0	808.0
11001	98.0	196.0	392.0	784.0
11010	95.0	190.0	380.0	760.0
11011	92.0	184.0	368.0	736.0
11100	89.0	178.0	356.0	712.0
11101	87.0	174.0	348.0	696.0
11110	85.0	170.0	340.0	680.0
11111	83.0	166.0	332.0	664.0
00000 (default)	81.0	162.0	324.0	648.0
00001	79.0	158.0	316.0	632.0
00010	77.5	155.0	310.0	620.0
00011	76.0	152.0	304.0	608.0
00100	74.5	149.0	298.0	596.0
00101	73.0	146.0	292.0	584.0
00110	71.5	143.0	286.0	572.0
00111	70.0	140.0	280.0	560.0
01000	69.0	138.0	276.0	552.0
01001	68.0	136.0	272.0	544.0
01010	67.0	134.0	268.0	536.0
01011	66.0	132.0	264.0	528.0
01100	65.5	131.0	262.0	524.0
01101	65.0	130.0	260.0	520.0
01110	64.5	129.0	258.0	516.0
01111	64.0	128.0	256.0	512.0

Linear Slope Control Scheme



Control Register Bit Definition for Linear Slope Mode.



Codes per step is determined by MS[1:0].

MS[1:0]	Code per step
00	One Step Mode
01	1 code
10	2 code
11	4 code

Step period is determined by ML[1:0] and ST[4:0].

ML[1:0]	Period[μs]
00	Refer to Linear slope selection table
01	Refer to Linear slope selection table
10	Refer to Linear slope selection table
11	Refer to Linear slope selection table

3. Two Step Control and Enhance Slope Control Set up Method

Protection off

Byte1(0xEC)								Byte2(0xA3)							
1	1	1	0	1	1	0	0	1	0	1	0	0	0	1	1

TSC, ESC and MC[1:0] setting

Byte1(0xA1)								Byte2							
1	0	1	0	0	0	0	1	0	0	0	ESC	TSC	1	MC1	MC0

ST[4:0] setting

Byte1(0xF2)								Byte2							
1	1	1	1	0	0	1	0	ST4	ST3	ST2	ST1	ST0	0	0	0

Protection on

Byte1(0xDC)								Byte2(0x51)							
1	1	0	1	1	1	0	0	0	1	0	1	0	0	0	1

Mode selection:

TSC: Two Step Control Mode (ESC=0)
1: Two step control mode
0: Normal operation mode

ESC: Enhance Slope Control Mode (TSC=0)
1: Enable ESC mode
0: Disable ESC mode

Note:
1. At ESC mode, ESC code=1 and TSC must be equal 0.
2. If ESC code=1 and TSC code=1, it get the TSC mode.

Two Step Control, Enhance Slope Control- step period selection table

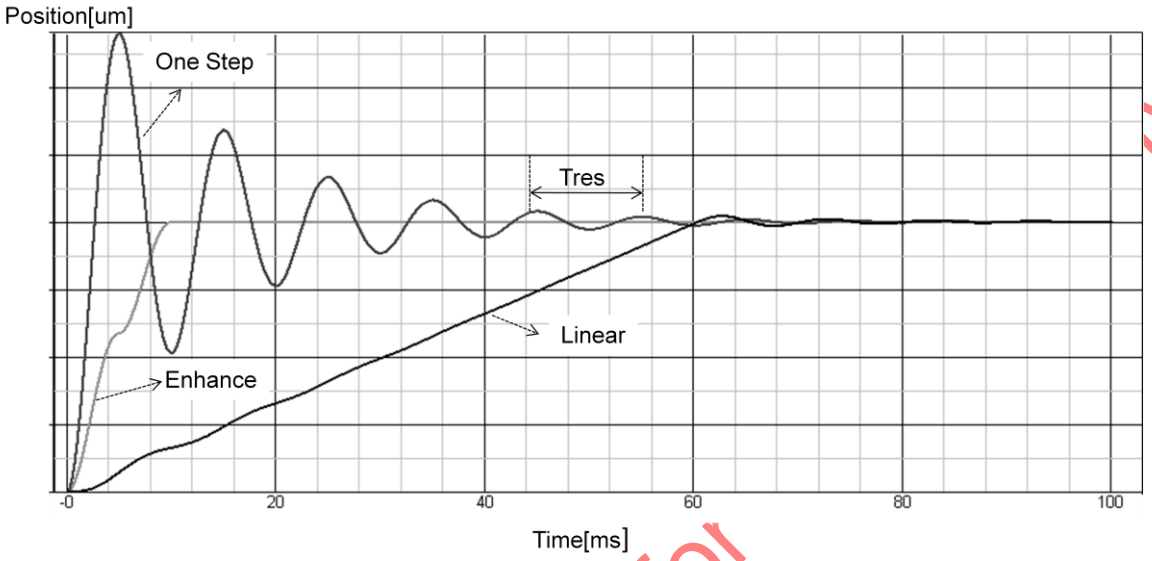
TSC & ESC step period is set by MC[1:0] and ST[4:0],

MC[1:0] default value is 2'b=01 and ST[4:0] default value is 5'b=00000.

Recommended that TSC & ESC step period is set Tres/2 (Tres= resonant period) Unit[ms]

Tres/2				
ST[4:0], 5'b	MC[1:0], 2'b			
	00	01	10	11
10000	21.25	10.63	5.31	2.66
10001	20.31	10.16	5.08	2.54
10010	19.53	9.77	4.88	2.44
10011	18.75	9.38	4.69	2.34
10100	18.13	9.06	4.53	2.27
10101	17.50	8.75	4.38	2.19
10110	16.88	8.44	4.22	2.11
10111	16.25	8.13	4.06	2.03
11000	15.78	7.89	3.95	1.97
11001	15.31	7.66	3.83	1.91
11010	14.84	7.42	3.71	1.86
11011	14.38	7.19	3.59	1.80
11100	13.91	6.95	3.48	1.74
11101	13.59	6.80	3.40	1.70
11110	13.28	6.64	3.32	1.66
11111	12.97	6.48	3.24	1.62
00000 (default)	12.66	6.33	3.16	1.58
00001	12.34	6.17	3.09	1.54
00010	12.11	6.05	3.03	1.51
00011	11.88	5.94	2.97	1.48
00100	11.64	5.82	2.91	1.46
00101	11.41	5.70	2.85	1.43
00110	11.17	5.59	2.79	1.40
00111	10.94	5.47	2.73	1.37
01000	10.78	5.39	2.70	1.35
01001	10.63	5.31	2.66	1.33
01010	10.47	5.23	2.62	1.31
01011	10.31	5.16	2.58	1.29
01100	10.23	5.12	2.56	1.28
01101	10.16	5.08	2.54	1.27
01110	10.08	5.04	2.52	1.26
01111	10.00	5.00	2.50	1.25

Comparison of One Step, Linear slope control and Enhance slope control with simulation performance.



Operation time and Tolerance coverage

Mode	Operation time (Note 6)	Actuator resonance period tolerance coverage (Note 7)(Note 8)
One step	-	-
LSC	-	-
TSC	0.5*Tres (Note 9)	±9%
ESC	1*Tres (Note 9)	±26%

Note 6: Isink current moving time.
Note 7: The error band of overshoot is moving stroke of ±10%.
Note 8: This is only design spec. Tolerance can be changed by mechanical characteristics of specific VCM.
Note 9: Tres is resonant period of the VCM.

WLCSP (Wafer Level Scale) Package Application

CSP Description:

Chip Scale Packages are defined as any package whose dimensions are no more than 20% larger than the die or chip that it contains. The Chip Scale Package represents the smallest possible footprint size in that the package is the same size as the die.

PCB Circuit Board Recommendations:

A summary of recommended PCB design parameters is shown in Table 1. Non-Solder mask defined (NSMD) pads are preferable, because the solder spheres will encompass the pad periphery wall as well as the pad surface, thereby providing extra strength for added solder joint integrity and better reliability.

Printed Circuit Board (PCB) Surface Finish Characteristics:

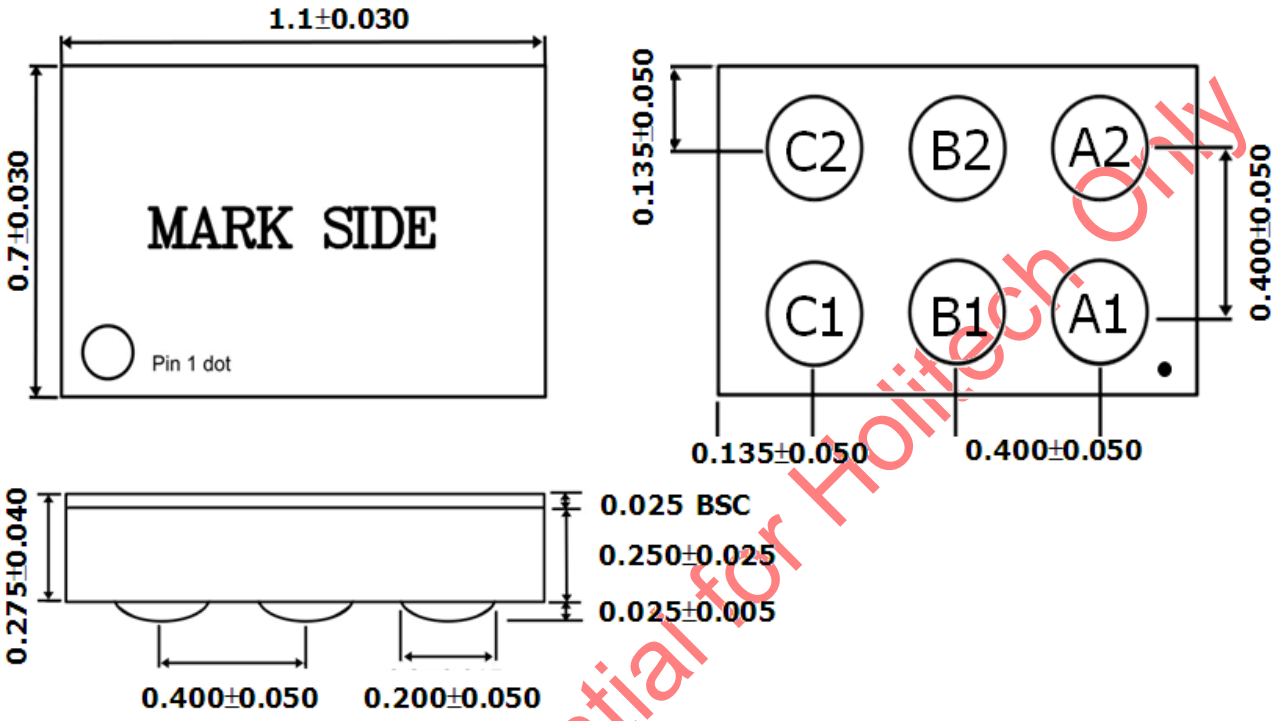
Organic Solder ability Preservative (OSP) finish recommended. Electronless nickel-immersion gold finish with gold thickness ranging from 0.05 microns to 0.127 microns may also be used. Because the PCB pad layout is critical to solder ball type package's board level reliability, the PCB pad layout must match to WLCSP's ball size.

Parameter	0.4mm Pitch 0.2mm Ball
Pad Size in PCB	0.25mm
Pad Shape	Round
Pad Definition	Non Solder Mask Defined Pads
Solder Mask Opening	0.3mm Round
Solder Stencil Thickness	0.125 ~ 0.150mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.330mm Round
Solder Flux Ratio	50/50 By Volume
Solder Paste Type	No Clean
Bond Trace Finish	OSP (Entek Cu Plus 106A)
Tolerance - Edge to Corner Ball	±50μm
Solder Ball Side Coplanarity	±20μm

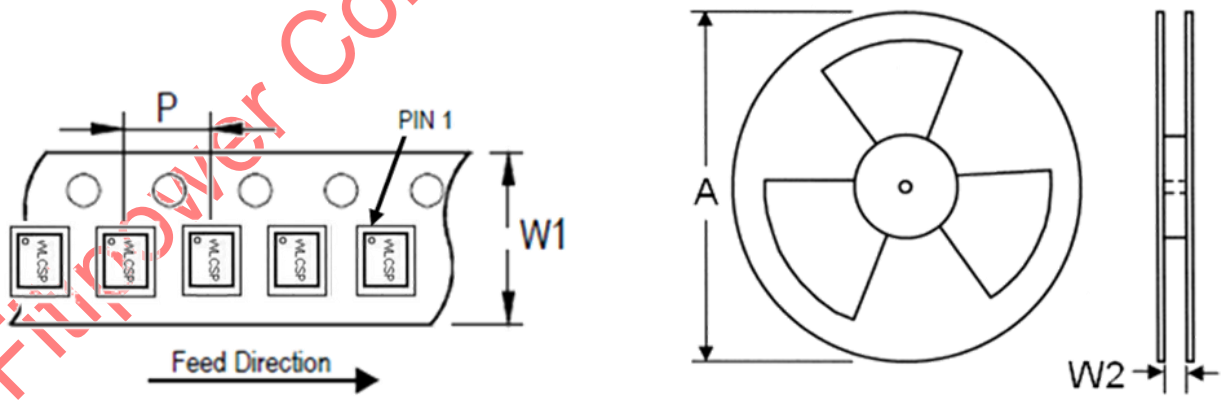
Table 1: PC Board Recommendations

Outline Information

FP5510 WLCSP-6 ball Package (0.7x1.1) (Unit: mm)



Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	9.5	400~1000	3,000